Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original) A charge pump circuit comprising:

a plurality of charge transfer transistors connected in series;

a plurality of capacitors each having one end connected to a corresponding connecting point of the charge transfer transistors;

a first clock driver for supplying clock pulses to the other end of the capacitor;

a second clock driver for supplying clock pulses to the other end of the capacitor and having higher driving capacity than the first clock driver; and

a clock driver control circuit for initiating operation of the first clock driver when the charge pump circuit starts operating and initiating operation of the second clock driver after a predetermined elapsed time, wherein an output voltage is obtained from one of the plurality of charge transfer transistors.

2. (Original) The charge pump circuit of claim 1, wherein the clock driver control circuit stops operation of the first clock driver at an end of the predetermined elapsed time.

3. (Currently Amended) The charge pump circuit of claim 1 ~~or claim 2~~, wherein the clock driver control circuit comprises a comparator which compares a voltage corresponding to the output voltage with a predetermined reference voltage and a control circuit which controls the first clock driver and the second clock driver according to an output signal of the comparator.

4. (Original) The charge pump circuit of claim 3, wherein the predetermined reference voltage is equal to a power supply voltage.

5. (Original) The charge pump circuit of claim 3, wherein the comparator is a hysteresis comparator.

6. (Original) The charge pump circuit of claim 3, wherein the voltage corresponding to the output voltage is obtained by dividing the output voltage by resistors.

7. (Currently Amended) The charge pump circuit of claim 1 ~~or claim 2~~, wherein the clock driver control circuit comprises a counter which counts the clock pulses and a control circuit which controls the first clock driver and the second clock driver according to an output signal of the counter.

8. (Original) A charge pump circuit comprising:

a first charge pump circuit comprising a first clock driver and a second clock driver having higher driving capacity than the first clock driver;

a second charge pump circuit comprising a third clock driver and a fourth clock driver having higher driving capacity than the third clock driver; and

a clock driver control circuit for initiating the first clock driver when the charge pump circuit starts operating, initiating the second clock driver after a first predetermined elapsed time and then initiating the third clock driver and initiating the fourth clock driver after a second predetermined elapsed time.

9. (Original) The charge pump circuit of claim 8, wherein the clock driver control circuit comprises a counter which counts clock pulses and a control circuit which controls the first clock driver, the second clock driver, the third clock driver and the fourth clock driver according to an output signal of the counter.

10. (New) The charge pump circuit of claim 2, wherein the clock driver control circuit comprises a comparator which compares a voltage corresponding to the output voltage with a predetermined reference voltage and a control circuit which controls the first clock driver and the second clock driver according to an output signal of the comparator.

11. (New) The charge pump circuit of claim 10, wherein the predetermined reference voltage is equal to a power supply voltage.

12. (New) The charge pump circuit of claim 10, wherein the comparator is a hysteresis comparator.

13. (New) The charge pump circuit of claim 10, wherein the voltage corresponding to the output voltage is obtained by dividing the output voltage by resistors.

14. (New) The charge pump circuit of claim 2, wherein the clock driver control circuit comprises a counter which counts the clock pulses and a control circuit which controls the first clock driver and the second clock driver according to an output signal of the counter.